ABSTRACT OF THE DISCLOSURE

A method and apparatus for determining the write delay time of a memory are provided. The apparatus includes a CPU, a memory, a north bridge chipset, a south bridge and a BIOS. The north bridge chipset, which is connected to the CPU and the memory, writes a pattern to the memory according to different write delay times. The BIOS reads the pattern stored in the memory, and checks the correctness of the read pattern to determine the common write delay time.

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